ATLAS

A NoC Generation and Evaluation Framework

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Abstract

What is it?

- ATLAS is a framework that automates various processes related to the design flow of Networks on Chip (NoCs).

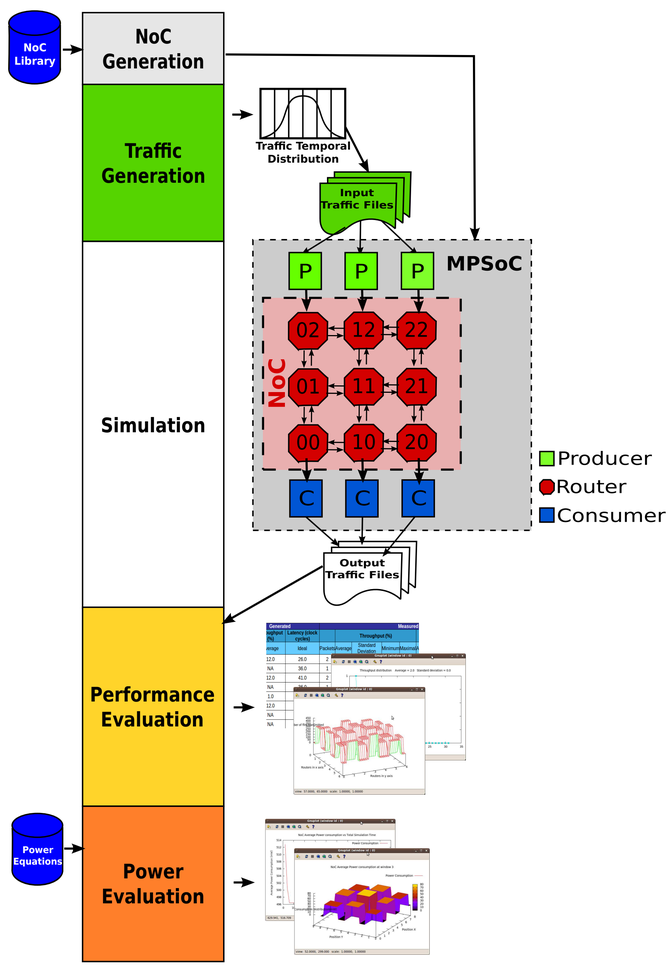
To whom is it addressed?

- Industrial: applications requiring high performance and/or low power consumption
- Academic: undergraduate or graduate advanced disciplines

Why use it?

- to automate generation and evaluation of NoCs
- to establish a good trade-off between the NoC architecture characteristics and the requirements of **performance** and **power consumption** of a given application

Design Exploration Flow



Tools

1) The **NoC Generation** tool generates the network according to the configuration of following parameters: network dimension; communication channel width; buffer depth; flow control; number of virtual channels; scheduling and routing algorithms. The generated NoC is described in VHDL and its test benches are described in SystemC.

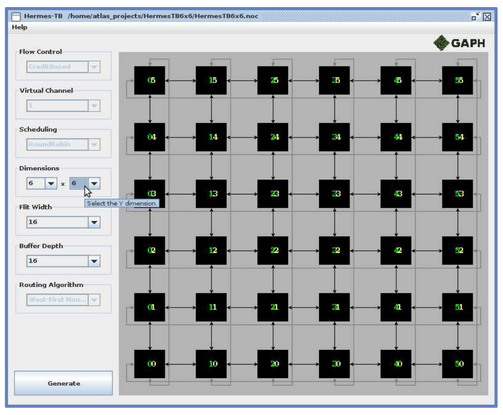


FIGURE 1: NoC Generation GUI.

2) The **Traffic Generation** tool produces different traffic patterns, for different injection rates and source/target pairs (e.g. random and complement). The packet timestamp (i.e. the moment in which a packet should be inserted into the NoC by a producer) is calculated according different temporal traffic distribution (e.g. normal, uniform and exponential).

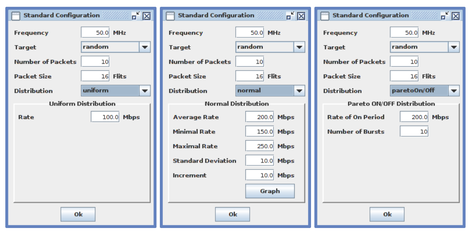


FIGURE 2: Windows for the configuration of the Uniform, Normal and Pareto On/Off traffic distributions.

3) The **Simulation** tool invokes a external VHDL/SystemC simulator: ModelSim. All generated traffic files are interpreted and injected to the NoC. During the simulation, consumers generate output files read by the traffic analysis module, when the simulation finishes, allowing to compute the latency and throughput for each packet.

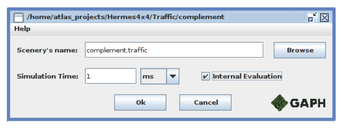


FIGURE 3: Window for controlling the NoC simulation tool.

4) The **Performance Evaluation** tool verifies if all packets were correctly received, and generates basic statistic data (e.g. a report file and charts) concerning time to deliver packets. The report file presents some traffic analysis results, such as: (i) total number of received packets, (ii) average time to deliver the packets, (iii) total time to deliver all packets and (iv) the average, minimal, maximal and standard deviation time to deliver a packet.

		Generated		Measured							Graphs	
			Throughput (%)	Latency (clock cycles)	Throughput (%)				Latency (clock cycles)			
Source	Target	Packets	Average	Ideal	Packets	Average	Standard Deviation	Minimum	Maximal	Average	Standard Deviation	Minimum	Maximal	Latency Distribution	Throughput Distribution
00	33	10	12.0	51.0	10	12.0	0.0	12.0	12.0	93.1	0.30	93.0	94.0	VIEW	VIEW
10	23	10	12.0	41.0	10	12.0	0.0	12.0	12.0	65.1	0.30	65.0	66.0	VIEW	VIEW
20	13	10	12.0	41.0	10	12.0	0.0	12.0	12.0	65.1	0.30	65.0	66.0	VIEW	VIEW
30	03	10	12.0	51.0	10	12.0	0.0	12.0	12.0	90.1	0.30	90.0	91.0	VIEW	VIEW
01	32	10	12.0	41.0	10	12.0	0.0	12.0	12.0	65.1	0.30	65.0	66.0	VIEW	VIEW
11	22	10	12.0	31.0	10	12.0	0.0	12.0	12.0	37.1	0.29	37.0	38.0	VIEW	VIEW
21	12	10	12.0	31.0	10	12.0	0.0	12.0	12.0	37.1	0.29	37.0	38.0	VIEW	VIEW
31	02	10	12.0	41.0	10	12.0	0.0	12.0	12.0	62.1	0.29	62.0	63.0	VIEW	VIEW
02	31	10	12.0	41.0	10	12.0	0.0	12.0	12.0	65.1	0.30	65.0	66.0	VIEW	VIEW
12	21	10	12.0	31.0	10	12.0	0.0	12.0	12.0	34.1	0.29	34.0	35.0	VIEW	VIEW
22	11	10	12.0	31.0	10	12.0	0.0	12.0	12.0	34.1	0.29	34.0	35.0	VIEW	VIEW
32	01	10	12.0	41.0	10	12.0	0.0	12.0	12.0	62.1	0.29	62.0	63.0	VIEW	VIEW
03	30	10	12.0	51.0	10	12.0	0.0	12.0	12.0	93.1	0.30	93.0	94.0	VIEW	VIEW
13	20	10	12.0	41.0	10	12.0	0.0	12.0	12.0	65.1	0.30	65.0	66.0	VIEW	VIEW
23	10	10	12.0	41.0	10	12.0	0.0	12.0	12.0	62.1	0.29	62.0	63.0	VIEW	VIEW
33	00	10	12.0	51.0	10	12.0	0.0	12.0	12.0	90.1	0.30	90.0	91.0	VIEW	VIEW
		160			160	12.0				63.78					

generated data — collected data — graphs

FIGURE 4: Global performance report.

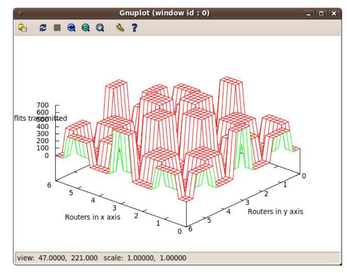


FIGURE 5: Number of flits transmitted in each channel.

5) The **Power Evaluation** tool uses an estimation model to generate NoC power results (e.g. power reports and charts). ATLAS contains a set of predefined equations annotated using a commercial power estimation tool (Synopsys PrimePower) [5]. These equations give the energy consumption and power dissipation according to the injection rate at each router port.

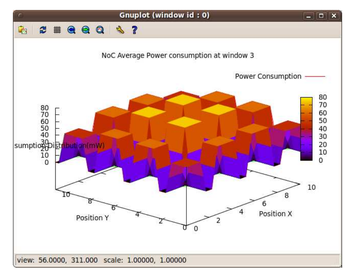


FIGURE 6: Average power consumption in each router(mW).

Type of NoCs

Parameters	Hermes [2][3]	Hermes TB	Hermes TU	Hermes SR	Hermes CRC
Topology	2D Mesh	2D Torus	1D Torus	2D Mesh	2D Mesh
Virtual Channels	1, 2 or 4	1	2	1 or 4	2
Flit Width	8, 16, 32 or 64			16	16
Buffer Depth	4, 8, 16 or 32				
Routing Algorithm	XY or West-first	West-first non miminal	Unidirectional XY	XY	XY
Scheduling Algorithm	Round Robin or Priority	Round Robin	Round Robin	Age Based	Round Robin
CRC	No	No	No	No	Yes
QoS	Yes	No	No	Yes	No

Conclusions

The main contribution of the ATLAS framework is to enable the designer to quickly evaluate the performance and power consumption of different NoC configurations, allowing optimize a NoC for a specific application or a set of them. NoCs generated by the ATLAS framework have been successfully prototyped in Xilinx **FPGAs** and have been used in industrial telecommunication applications [6]. An **ASIC** prototype (65 nm) is being developed.

ATLAS is written in Java, allowing its execution in different hardware/software platforms. It also has an intuitive GUI which helps the designer to configure the NoC. The ATLAS framework is an active development project, with contributors and users from different countries, where new features are being included continuously. The latest version of ATLAS is freely available at [1] for download. The GAPH website [7] has more information about other NoC-related tools such as CAFES (task mapping tool for NoC-based MPSoCs) and HemPS (MPSoC generator).

Some References

[1] ATLAS main page. **https://corfu.pucrs.br/redmine/projects/atlas**

[2] F. Moraes, et al. Hermes: an infrastructure for low area overhead packet-switching networks on chip. Integration, VLSI Journal, 38:69-93, October 2004.

[3] A. Mello, et.al. MultiNoC: A Multiprocessing System Enabled by a Network on Chip. Best Conceptual Design in DATE'05, 234-239, 2005.

[4] L. Tedesco, et al. Traffic generation and performance evaluation for mesh-based NoCs. In SBCCI'05, 184-189, 2005.

[5] G. Guindani, et al. NoC power estimation at the rtl abstraction level. VLSI'08, 0:475-478.

[6] F. Moraes, et al. MOTIM: an industrial application using NoCs. SBCCI 2008.

[7] GAPH website. **http://www.inf.pucrs.br/~gaph**